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parallel "control words" 1994 - 2001 Search

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All Results
K Rayner
S Scott
H van der Bij
R Minnich
S Kim

Multi bit per pixel compression/decompression using **parallel** encoded streams - all 3 versions »
F Blurfrushan, RE Joiner, SC Kang - US Patent 5,754,746, 1998 - Google Patents
... DECOMPRESSION USING **PARALLEL** ... and for combining said instructions and mask data onto
a third line and into a series of first multi-bit **control words**, one first ...
Cited by 14 - Related Articles - Web Search

Voltage multiplier using switched capacitance technique - all 3 versions »
MJ Jansen - US Patent 5,491,623, 1996 - Google Patents
... SOb-i requiring a set of **parallel** control signals ai are replaced with two multiplexers coupled to a digital control bus 82 to receive digital **control words**. ...
Cited by 18 - Related Articles - Web Search

S-LINK, a data link interface specification for the LHC era - all 5 versions »
HC van der Bij, RA McLaren, O Boyle, G Rubin - Nuclear Science, IEEE Transactions on, 1997 - ieeexplore.ieee.org
... read-out electronics and input buffers, to work in **parallel** with the ... The physical link provides transfer of event data and **control words**, error detection ...
Cited by 27 - Related Articles - Web Search

Massively **parallel** processing system using two data paths: one connecting router circuit to the ... - all 2 versions »
RE Kessler, SM Oberlin, SL Scott - US Patent 5,864,738, 1999 - Google Patents
Page 1. [54] MASSIVELY **PARALLEL** PROCESSING SYSTEM USING TWO DATA PATHS ... ' .' , UI
XT ^ I " mr ir T *• **Parallel** and Distributed Systems, vol. 4, No. 12, pp. ...
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The memory-integrated network interface - all 6 versions »
R Minnich, D Burns, F Hady, DSR Center, NJ ... - Micro, IEEE, 1995 - ieeexplore.ieee.org
... The same dual-port SRAM used to hold the VC **control words** also holds a mnsmit and receive AALS CRC value for each VC. ... (This occurs in **parallel** with the network ...
Cited by 48 - Related Articles - Web Search

Error detection for **parallel** data transfer between a processor and a peripheral device by comparing ... - all 3 versions »
M Myran... - US Patent 5,506,958, 1996 - Google Patents
... then be latched into peripheral controller 16 via latch 17, and **control words** will be ... has occurred, computer 12 outputs data 65 through **parallel** port interface ...
Cited by 11 - Related Articles - Web Search

System and method for sending multiple data signals over a serial link - all 5 versions »
S Kim, DD Lee, DK Jeong... - US Patent 5,835,498, 1998 - Google Patents
Page 1. US005835498A United States Patent Kim et al. [73] Assignee: Silicon Image, Inc., Cupertino, Calif. [21] Appl. No.: 664,136 [22] Filed: Jun. 14, 1996 ...

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Wideband interference suppressor in a phased array radar - all 2 versions »
K Chang, F Beltran, F Steudel - US Patent 5,592,178, 1997 - Google Patents
Page 1. United States Patent Chang et al. US005592178A [ii] Patent Number: [45] DateofPatent: [54] WIDEBAND INTERFERENCE SUPPRESSOR IN A PHASED ARRAY RADAR ...
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Multipath torus switching apparatus - all 2 versions »
HT Olnowich, AR Williams - US Patent 5,408,646, 1995 - Google Patents
Page 1. US005408646A United States Patent Olnowich et al. [ii] Patent Number: [45] Date of Patent: [54] MULTIPATHTORUSSWITCHING APPARATUS ...
Cited by 24 - Related Articles - Web Search

[PDF] Contextual strength does not modulate the subordinate bias effect: Evidence from eye fixations and ... - all 2 versions »
KS Binder, K Rayner - Psychonomic Bulletin and Review, 1998 - psychonomic.org
... the subordinate sense (the subordinate bias effect) than on the unambiguous **control words** or on the ... Sentence perception as an interactive, **parallel** process. ...
Cited by 74 - Related Articles - View as HTML - Web Search

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parallel "control words" Search

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All Results
S Browne
J Dongarra
N Garner
G Ho
P Mucci

Graphemes are perceptual reading units - all 8 versions »
A Rey, JC Ziegler, AM Jacobs - Cognition, 2000 - Elsevier
... the multi-letter grapheme **unit** EA will ... model that contained graphemes as intermediate **functional units**. ... could be to increase **parallel** processing (Laberge & ...
Cited by 28 - Related Articles - Web Search

A transformation-based method for loop folding - all 4 versions »
TF Lee, ACH Wu, YL Lin, DD Gajski - Computer-Aided Design of Integrated Circuits and Systems, ..., 1994 - ieeexplore.ieee.org
... into each control step, fewer **functional units** are sufficient ... for each scheduled control step in the control **unit**. ... is increased from four to six **control words**. ...
Cited by 40 - Related Articles - Web Search

A Portable Programming Interface for Performance Evaluation on Modern Processors - all 15 versions »
S Browne, J Dongarra, N Garner, G Ho, P Mucci - International Journal of High Performance Computing ..., 2000 - hpc.sagepub.com
... for measuring how heavily the different **functional units** are being ... A functional **unit** is idle if it has no ... for devel- opment environment for **parallel** programs. ...
Cited by 189 - Related Articles - Web Search

Instruction compression and decompression system and method for a processor - all 4 versions »
RG Miller, LA Cardillo, JG Mathieson, ER Smith - US Patent 5,819,058, 1998 - Google Patents
... **ROUTING** SELECT LOGIC ... possible to fully utilize all of the multiple **functional units** during every ... processing units may be connected together in **parallel** so that ...
Cited by 22 - Related Articles - Web Search

Design and VLSI implementation of an address generation coprocessor - all 9 versions »
PT Hulina, LD Coraor, L Kurian, E John - Computers and Digital Techniques, IEE Proceedings-, 1995 - ieeexplore.ieee.org
... in microelectronic technology, the addition of **functional units** to the ... by a simple **parallel** input **parallel** output up ... Fig. 6 Reflected address generation **unit** ...
Cited by 3 - Related Articles - Web Search

Architecture and implementation of a single-chip programmabledigital television and media processor
S Dutta, D Singh, V Mehra, P Semicond, CA ... - Signal Processing Systems, 1999. SiPS 99. 1999 IEEE Workshop ..., 1999 - ieeexplore.ieee.org
... The MMI **unit** manages the interface between TM ... are optionally guarded and the **parallel**
instructions (operations ... of 27 **functional units** that include the integer ...
Cited by 4 - Related Articles - Web Search

Centralized performance monitoring architecture - all 2 versions »

S Agrawal, AF Glew, PG Franklin, R Spotten - US Patent 5,881,223, 1999 - Google Patents
... RP3 Performance Monitoring Hard -ware," **Parallel** Computing Sys ... The **functional units**
of segment 295 (not shown) are ... Control **unit** 200 generates **control words** that ...
Cited by 4 - Related Articles - Web Search

... having primary integer execution **unit** and supplemental integer execution **unit** for performing out-of ... - all 3 versions »
EA Sowadsky, L Widigen, DL Puziol, KS Van Dyke... - US Patent 5,675,758, 1997 - Google Patents
... purpose of this discussion, instructions can be units capable of performing **parallel** speculative execution. ... **unit** (AP ... tha are broadcast to the **functional units**. ...
Cited by 3 - Related Articles - Web Search

... via **parallel** out-of-order execution of adds and moves in a supplemental integer execution **unit** - all 6 versions »
EA Sowadsky, L Widigen, DL Puziol, KS Van Dyke - US Patent 5,802,339, 1998 - Google Patents
... **functional units** in the processor ... preparation **unit** without passing through the operations bus, wherein the add/move **unit**, operates in **parallel**, and out ...
Cited by 2 - Related Articles - Web Search

The Institute of Precision Mechanics and Computer Technology and the El'brus family of high-speed ... - all 9 versions »
P Wolcott, MN Dorojevets - IEEE Annals of the History of Computing, 1998 - doi.ieeecs.org
... use of special-purpose registers and **control words** to manage ... an indexation **unit**. ... architectures are not well-suited to feed multiple, **parallel functional units**. ...
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"functional units" parallel router OR Search

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parallel "control words" "functional units" "rou 1994 - 2001 Search

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All Results
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D Gajski
A Rey
A Wu
Y Lin

Graphemes are perceptual reading units - all 8 versions »
A Rey, JC Ziegler, AM Jacobs - Cognition, 2000 - Elsevier
... O more often in OF than in **control words**. ... model that contained graphemes as intermediate
functional units. ... could be to increase **parallel** processing (Laberge & ...
Cited by 28 - Related Articles - Web Search

Instruction compression and decompression system and method for a processor - all 4 versions »
RG Miller, LA Cardillo, JG Mathieson, ER Smith - US Patent 5,819,058, 1998 - Google Patents
... utilize all of the multiple **functional units** during every ... The invention may also **route** said decompressed variable ... may be connected together in **parallel** so that ...
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A transformation-based method for loop folding - all 4 versions »
TF Lee, ACH Wu, YL Lin, DD Gajski - Computer-Aided Design of Integrated Circuits and Systems, ..., 1994 - ieeexplore.ieee.org
... into each control step, fewer **functional units** are sufficient ... is four clock cycles, and a data-**path** needs at ... cost is increased from four to six **control words**. ...
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Peripheral memory interface controller as a cache for a large data processing system - all 3 versions »
TM Steckler, DA Gryger, RH Tickner - US Patent 5,446,844, 1995 - Google Patents
... queue 36 are the main **functional units** of the ... 3, to present **control words** and any associated address ... In **parallel** with this operation, information passes to ...
Cited by 11 - Related Articles - Web Search

Pipeline throughput via **parallel** out-of-order execution of adds and moves in a supplemental integer ... - all 6 versions »
EA Sowadsky, L Widigen, DL Puziol, KS Van Dyke - US Patent 5,802,339, 1998 - Google Patents
... SYSTEM units capable of performing **parallel** speculative execution. ... that are broadcast to the **functional units**. Each instruction ... unencoded) **control words**. ...
Cited by 2 - Related Articles - Web Search

Semiconcurrent error detection in data paths - all 10 versions »
A Antola, F Ferrandi, V Piuri, M Sami - Computers, IEEE Transactions on, 2001 - ieeexplore.ieee.org
... a sequence of □k x control steps over which the nominal schedule is repeated □ times; allocation of **functional units** in the nominal data **path** is given. ...
Cited by 21 - Related Articles - Web Search

High-speed 2-D convolution with a custom computing machine - all 7 versions »
JB Peterson, PM Athanas - The Journal of VLSI Signal Processing, 1996 - Springer

... Each interconnection represents a 36-bit data **path**. ... the nec- essary data to the appropriate **functional units** is an ... the host passes special **control words** to the ...
Cited by 5 - Related Articles - Web Search

[PDF] Efficient SoC design with homogeneous processor arrays - all 3 versions »
M Zajc, R Sernec, J Tasic - CAN J ELECTR COMPUT ENG, 2001 - ldos.fe.uni-lj.si
... The number of **functional units** within the scalar ... The whole **parallel** processor ensemble
is controlled via ... wide horizontal microcode **control words** for processing ...
Related Articles - View as HTML - Web Search

Rapid pipeline control using a control word and a steering word - all 3 versions »
TW Lynch... - US Patent 5,930,492, 1999 - Google Patents
... word specifies the **routing** of the instruction through the pipeline stages. Many pipeline modifications may be made by modifying the **control words** and steering ...
Cited by 7 - Related Articles - Web Search

Method and apparatus for controlling configuration memory contexts of processing elements in a ... - all 3 versions »
E Mirsky, R French, I Eslick - US Patent 5,915,123, 1999 - Google Patents
... al; "A High-Performance Microarchitecture with Hardware-Programmable **Functional Units**"; Micro-27 ... Element for a High Performance Massively **Parallel** SIMD System ...
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E Mirsky
P Pacheco
D Culler
J Grainger
A DeHon

... computing architecture with configurableinstruction **distribution** and deployable resources - all 3 versions »
E Mirsky, A DeHon - FPGAs for Custom Computing Machines, 1996. Proceedings. IEEE ..., 1996 - ieeexplore.ieee.org
... these two operations proceed in **parallel** The BFU ... 1: MATRIX I3FU Level—I .5oe **Control**
Byte Register on A,B Ports Only Configuration Configuration **Word** A **Word** ...
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The NAPA Adaptive Processing Architecture - all 7 versions »
CR Rupp, M Landguth, T Garverick, E Gomersall, H ... - IEEE Symposium on Field-Programmable Custom Computing ..., 1998 - doi.ieeecomputersociety.org
... The common ToggleBus **control** bus "C" is used to ... supports general bit-level and **word**-level "data ... both SIMD and MIMD style **parallel** processing approaches ...
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[BOOK] **Parallel** Programming with MPI - all 3 versions »
PS Pacheco - 1997 - books.google.com
... 8.4.2 Model Problem 161 8.4.3 **Distribution** of the Input 162 ... 307 13.8 The Last **Word** on Point-to-Point Communication 309 13.9 Summary ... Ch **Parallel** Algorithms 315 ...
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Realization of a programmable **parallel** DSP for high performance image processing applications - all 10 versions »
JP Wittenburg, W Hinrichs, J Kneip, M Ohmacht, M ... - Design Automation Conference, 1998 - doi.ieeecomputersociety.org
... 48 * 48 **words** / 16 bit TEST AND DEBUG INTERFACE ... So, our experience in the **parallel**
implementation of image processing application and ... Instruction Cache **Control** ...
Cited by 12 - Related Articles - Web Search

Singulars and Plurals in Dutch: Evidence for a **Parallel** Dual-**Route** Model - all 3 versions »
RH Baayen, T Dijkstra, R Schreuder - Journal of Memory and Language, 1997 - Elsevier
... tion of our **parallel** dual-**route** model ... three items of the same type (either **word** or pseudoword ... in sequence, and that 97 participants, the **distribution** of reaction ...
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... and Function in the Lexical System: Insights from Distributed Models of **Word** Reading and Lexical ... - all 8 versions »
DC Plaut - Cognitive Models of Speech Processing: Psycholinguistic and ..., 1998 - books.google.com
... adopted by researchers employing connectionist/**parallel** distributed processing ... with the core tenet of dual-**route** theories. ... graphemes contained in the **word** to 1 ...
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[BOOK] **Parallel** computer architecture - all 3 versions »

DE Culler, JP Singh - 1999 - eng.ku.ac.th
... Shared Virtual Memory.....638 9.4.4 Access **Control** through Language ... 652 9.6 Implications for **Parallel** Software ...
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Advanced **parallel** array processor I/O connection - all 2 versions »
TN Barker, CA Collins, MC Dapp, JW Dieffenderfer, ... - US Patent 5,617,577, 1997 - Google Patents
... Alleyne et al., "A Bit-**Parallel**, **Word-Parallel**, Massively **Parallel** ... Arithmetic in a Massively-**Parallel** Associative Processor ... Richter and G. Raupp, "**Control** of a ...
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Distributed **parallel** object-oriented environment for traffic simulation (POETS) - all 2 versions »
SL Mabry, JL Gaudiot - Proceedings of the 26th conference on Winter simulation, 1994 - portal.acm.org
... timing mechanism is provided for **control** of the ... general **parallel** simulations of real-world events ... Obvious objectives in **parallel** and distributed simulation are ...
Cited by 7 - Related Articles - Web Search

Digitally programmable radio modules for navigation systems - all 3 versions »
WC Phillips, MV Pascale, RW Minarik, KM Schmidt, ... - US Patent 5,909,193, 1999 - Google Patents
... due to the complexity of signal **distribution** and switching ... including AIR TRAF- FIC **CONTROL** RADAR BEACON ... or more sequential and/or **parallel** instruction processors ...
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STIC SEARCH NOTES
P. 1 of 28

PATENT ABSTRACTS

[File 347] **JAPIO** Dec 1976-2007/Jun(Updated 070926)
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[File 350] **Derwent WPIX** 1963-2007/UD=200801
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**File 350: English-language translations of Chinese Utility Model registrations are available starting with update 200769.*

; d s

Set	Items	Postings	Description
S1	4602	39794	S CONTROL()WORD? ? OR ROUT???(2N)INSTRUCTION? ?
S2	39345	247936	S (ROUT??? OR STEER???)(2N)(UNIT? ? OR PART? ? OR APPARATUS OR APPTS OR ELEMENT? ?)
S3	12	31	S FUNTIONAL(2N)(UNIT? ? OR PART? ? OR APPARATUS OR APPTS OR ELEMENT? ?)
S4	1485604	9090684	S (LOGIC? OR LOOKUP? OR LOOK()UP? ? OR SHIFT??? OR STORAGE)()(UNIT? ? OR PART? ? OR APPARATUS? OR APPTS OR ELEMENT? ?) OR ALU OR ALUS OR MEMORY OR BUFFER? ?
S5	114	722	S S1(5N)(PARALLEL? OR SIMULTANEOUS? OR SAME()TIME)
S6	102456	675029	S S3:S4(3N)(CONFIGUR? OR SELECT? OR ARRANG? OR ORDER?)
S7	2	30	S S5 AND S2 AND S6
S8	17	240	S S5 AND S6
S9	15	222	S S8 NOT S7
S10	15	222	S S9 NOT AD=20011107:20080808/PR
S11	48718	187429	S ARCHITECTURE
S12	2927	47502	S S11 AND S6
S13	36	1202	S S12 AND S1
S14	36	1202	S S13 NOT (S7 OR S10)
S15	26	715	S S14 NOT AD=20011107:20080808/PR
S16	14	534	S S15 AND (ROUT? OR STEER?)
S17	48	305	S CONTROL()WORD? ?(5N)PARALLEL?
S18	38	246	S S17 NOT (S7 OR S10 OR S14)
S19	30	209	S S18 NOT AD=20011107:20080808/PR
S20	150	716	S DATA()STEERING
S21	2	56	S S20 AND CONTROL()WORD? ?

7/5/1 (Item 1 from file: 350) **Links**
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0008113846 *Drawing available*
WPI Acc no: 1997-212460/199719
XRPX Acc No: N1997-175327
Multiple instruction selection and buffering unit for CPU execution - has decoder generating bundle instruction indicating whether even and odd instruction pair can be executed simultaneously with selector routing instructions to operational units
Patent Assignee: HEWLETT-PACKARD CO (HEWP)
Inventor: DELANO E R

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5617549	A	19970401	US 1992957344	A	19921006	199719	B
			US 1994296989	A	19940826		

Priority Applications (no., kind, date): US 1992957344 A 19921006; US 1994296989 A 19940826

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 5617549	A	EN	17	7	Continuation of application	US 1992957344

Alerting Abstract US A
The instruction selection unit has an address unit fetching even and odd instructions from a memory system. A decoder generates a bundle signal indicating whether a pair of even and odd instructions can be executed simultaneously. First and second busses transport the even instructions received from the memory system. Third and fourth busses transport the odd instructions received from the memory system. A first master/slave register coupled to the second bus, stores the even instructions. A second master/slave register, coupled to the third bus, stores the odd instructions. A first selector responsive to the bundle signal, selects at an output terminal, an even instruction from either the first bus or the first master/slave register, and at another one of the output terminals, an odd instruction from either the fourth bus or the second register.
A second selector roots aligned even and odd instructions that can be bundled, misaligned even and odd instructions that can be bundled or individual even or odd instructions that cannot be bundled from the first selector to specific operational units located in the execution unit. Control logic coupled to the first and second selectors generates signals that control which input terminals are selected by the first and second selectors.
ADVANTAGE - Provides high flexibility when switching between execution of single and bundles instructions. Incurs no penalty cycle when switching between single and bundled instructions or aligned and misaligned bundles.

7/3,K/2 (Item 2 from file: 350) **Links**
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0006212400 *Drawing available*
WPI Acc no: 1993-001393/199301
XRPX Acc No: N1993-000917
Data processing appts. - uses single instruction with FIFO buffer to distribute operating codes to multiple processors
Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG); LAB ELECTRONIQUE PHILIPS (PHIG); LAB ELECTRONIQUE PHILIPS SAS (PHIG); PHILIPS ELECTRONICS NV (PHIG); PHILIPS GLOEILAMPENFAB NV (PHIG); US PHILIPS CORP (PHIG)
Inventor: DURANTON M

Patent Family (5 patents, 3 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 520572	A1	19921230	EP 1992201842	A	19920623	199301	B
FR 2678402	A1	19921231	FR 19918064	A	19910628	199309	E
US 5675776	A	19971007	US 1992904732	A	19920625	199746	E
			US 1994353584	A	19941212		
EP 520572	B1	19990512	EP 1992201842	A	19920623	199923	E
DE 69229145	E	19990617	DE 69229145	A	19920623	199930	E
			EP 1992201842	A	19920623		

Priority Applications (no., kind, date): FR 19918064 A 19910628

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
EP 520572	A1	FR	23	9		
Regional Designated States,Original	DE FR GB					
US 5675776	A	EN	12	9	Continuation of application	US 1992904732
EP 520572	B1	FR				
Regional Designated States,Original	DE FR GB					
DE 69229145	E	DE			Application	EP 1992201842
					Based on OPI patent	EP 520572

Original Publication Data by Authority...**Claims:**codes; an operational unit comprising a plurality of operational means executing the operation codes in **parallel**; and **routing** circuitry **for routing** the operation codes from the central instruction decoder to the operational units for parallel execution, the **routing circuitry** comprising at least one FIFO type **memory**, **arranged** between at least one of the operational **units** and the **central** instruction decoder, said at least one FIFO type memory being for providing operation codes, under control of the routing circuitry, to the at least **one of** the operational **units**, wherein the **routing** circuitry **comprises** means for controlling access to said the at least one FIFO type memory by means...

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0007728353 *Drawing available*
WPI Acc no: 1996-351647/199635
XRPX Acc No: N1996-296519
Event queue control circuit for communication control processor - has read address circuits updating event queue performed in write-in address circuits detected by comparator
Patent Assignee: NIPPON TELEGRAPH & TELEPHONE CORP (NITE)
Inventor: MARUYAMA M; YAMASHITA M

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
JP 8166886	A	19960625	JP 1994310874	A	19941214	199635	B

Priority Applications (no., kind, date): JP 1994310874 A 19941214

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
JP 8166886	A	JA	8	5	

Alerting Abstract JP A
The circuit has a buffer (9) which stores the address of other buffers. A control word memory stores the control word of an interrupted processing demand which is secured from the buffer using the other buffers. A write-in circuit (3-1,3-2,3-3) which holds a first write-in and a last write-in control word of the **control word memory** is **arranged** in **parallel** with a read circuit (4-1,4-2,4-3) which holds a first and a last read control word of the control word memory.
The respective circuit connects to a write-in and a read comparator (6-1,6-2) which detects the write-in and read coincidence, respectively. The write-in circuits performs event queue processing. A processor (8) inputs the control word of an interrupted processing demand to a control circuit (5). The control circuit returns the used buffer to the management buffer when the comparator shows coincidence which updates read address circuits.
ADVANTAGE - Provides high efficiency on memory processing. Updates read address with queue address. Performs effective and practical usage of memory resources.

10/3,K/3 (Item 3 from file: 350) **Links**
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0012911384 *Drawing available*
WPI Acc no: 2002-413840/200244
XRPX Acc No: N2002-325280
Control signal generation circuit for testing high frequency synchronous digital circuits, particularly memory chips, has a built outside self test comprising an eight stage shift register with parallel loading inputs and serial outputs
Patent Assignee: ERNST W (ERNS-I); INFINEON TECHNOLOGIES AG (INFN); KRAUSE G (KRAU-I); KUHN J (KUHN-I); LUPKE J (LUPK-I); MULLER J (MULL-I); POCHMULLER P (POCH-I); SCHITTENHELM M (SCHI-I)
Inventor: ERNST W; KRAUSE G; KUHN J; LUEPKE J; LUPKE J; MUELLER J; MULLER J; POCHMULLER P; POECHMUELLER P; SCHITTENHELM M

Patent Family (4 patents, 2 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20020010878	A1	20020124	US 2001907784	A	20010718	200244	B
DE 10034851	A1	20020214	DE 10034851	A	20000718	200244	E
US 6839397	B2	20050104	US 2001907784	A	20010718	200503	E
DE 10034851	B4	20060608	DE 10034851	A	20000718	200639	E

Priority Applications (no., kind, date): DE 10034851 A 20000718; US 2001907784 A 20010718

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 20020010878	A1	EN	5	1	

Original Publication Data by Authority...**Original Abstracts:**has connected to its parallel loading inputs p logical gates which logically combine a static **control word** with a dynamic n-position **test** word. The combined logical value is loaded into the shift register at a low-frequency... ...**Claims:**A circuit configuration for generating control signals for testing high-frequency synchronous digital circuits, including **memory** chips, the circuit **configuration** comprising: a p-stage shift register clocked at a clock frequency corresponding to a high... ... inputs of said p-stage shift register, said logical gates receive and logically combine a **static** control word with **an** n-position dynamic test word in order to load a combined logical value into said... ... A circuit configuration for generating control signals for testing high-frequency synchronous digital circuits, including **memory** chips, the circuit **configuration** comprising: a p-stage shift register clocked at a clock frequency corresponding to a high... ... and logically combine a static control word with an n-position dynamic test word in **order** to load a **combined** logical value into **said** p-stage shift register at a low-frequency loading clock rate so that, at said...

10/5/14 (Item 14 from file: 350) **Links**
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0005720392 *Drawing available*
WPI Acc no: 1991-334186/199146
XRPX Acc No: N1991-256093
Parallel processing system with slice-wise communications arrangement - includes processing nodes with memory, transposer module, and router node, which are controlled in parallel and interconnected by links
Patent Assignee: THINKING MACH CORP (THIN-N); THINKING MACHINES CORP (THIN-N)
Inventor: BROMLEY H M

Patent Family (6 patents, 3 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 456201	A	19911113	EP 1991107437	A	19910507	199146	B
CA 2041893	A	19911109				199205	E
US 5247613	A	19930921	US 1990520701	A	19900508	199339	E
EP 456201	A3	19930303	EP 1991107437	A	19910507	199349	E
EP 456201	B1	19960918	EP 1991107437	A	19910507	199642	E
DE 69122161	E	19961024	DE 69122161	A	19910507	199648	E
			EP 1991107437	A	19910507		

Priority Applications (no., kind, date): US 1990520701 A 19900508

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
EP 456201	A	EN				
Regional Designated States,Original	DE FR GB					
CA 2041893	A	EN				
US 5247613	A	EN	17	4		
EP 456201	A3	EN				
EP 456201	B1	EN	18			
Regional Designated States,Original	DE FR GB					
DE 69122161	E	DE			Application	EP 1991107437
					Based on OPI patent	EP 456201

Alerting Abstract EP A
The massively parallel processing system comprises a number of processing nodes controlled in parallel by a controller. The processing nodes are inter-connected by a number of communications links. Each processing node comprises a memory, a transposer module and a router node. The memory stores data in slice format. The transposer module is connected to the memory and generates transpose data words of selected ones of the data slices from the memory. The router mode is connected to the transposer module and to the communication links and transfers transposed data words over the communications links to transfer the data slices between processing nodes.
The controller controls the memories transposer modules and router nodes of the processing nodes in parallel to facilitate transfer of data slices among the processing nodes in unison.
ADVANTAGE - Improved rate of data transmission. @(15pp Dwg.No.1/3)@

19/3,K/19 (Item 16 from file: 350) **Links**
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0005431665 *Drawing available*
WPI Acc no: 1991-030834/199105
XRPX Acc No: N1991-023868
Synchronous one-bit mesh processor - has circuitry enabling selected processors to respond to control information indicative of logical function to be performed
Patent Assignee: HUGHES AIRCRAFT CO (HUGA)
Inventor: MUMME M A

Patent Family (7 patents, 12 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 410435	A	19910130	EP 1990114298	A	19900726	199105	B
AU 199059930	A	19910131				199112	E
CA 2021192	A	19910129				199116	E
EP 410435	A3	19920226	EP 1990114298	A	19900726	199324	E
IL 95192	A	19940227	IL 95192	A	19900726	199419	E
KR 199400293	B1	19940114	KR 199011437	A	19900727	199445	E
US 5379444	A	19950103	US 1989386933	A	19890728	199507	E
			US 1992970978	A	19921103		
			US 1993106771	A	19930811		
			US 1994255294	A	19940607		

Priority Applications (no., kind, date): US 1994255294 A 19940607; US 1993106771 A 19930811; US 1992970978 A 19921103; US 1989386933 A 19890728

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
EP 410435	A	EN				
Regional Designated States,Original	CH DE ES FR GB IT LI SE					
CA 2021192	A	EN				
EP 410435	A3	EN				
IL 95192	A	EN				
US 5379444	A	EN	10	6	Continuation of application	US 1989386933
					Continuation of application	US 1992970978
					Continuation of application	US 1993106771

Equivalent Alerting Abstract ...as one of the one-bit inputs to the logic unit. A control provides a **control word** in **parallel** to all of the number of single bit processor cells, such that each single bit... ...operation specified by the control word. The number of single bit processor cells operate in **parallel** pursuant to receiving the **control word** and subsequent selective enablement by the selector... Original Publication Data by Authority...**Claims:**one-bit logic outputs; - control means (20) for providing a control word to each of **said processors** (Pij) in **parallel** and for providing a selection signal indicative of selected ones of said processors (Pij); and... ... outputs from other ones of said plurality of processor cells; control means for providing a **control word** in **parallel** to all of said plurality of single bit processor cells, such that each single **bit processor** cell **receives** said **control word** which specifies a logical operation; and selection means for enabling selected processor cells to perform... ... specified by said control word; whereby said plurality of single bit processor cells operate in **parallel** pursuant to receiving said **control word and** subsequent selective enablement by said selection means.

19/5/27 (Item 24 from file: 350) **Links**
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0002457929
WPI Acc no: 1982-B5682E/198207
Data processor peripheral control system - has specialised control-word memory relieving processor of responsibility for time-critical operations
Patent Assignee: COMPUTER GES KONSTANZ (COMP-N)
Inventor: DENK H; EGGER A; KOHMANN L

Patent Family (3 patents, 10 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 45438	A	19820210	EP 1981105746	A	19810721	198207	B
DE 3029136	A	19820325	DE 3029136	A	19800731	198213	E
DE 3029136	C	19820603	DE 3029136	A	19800731	198223	E

Priority Applications (no., kind, date): DE 3029136 A 19800731

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
EP 45438	A	DE	11		
Regional Designated States,Original	AT BE CH FR GB IT LI NL SE				

Alerting Abstract EP A
A **control word** memory is connected **parallel** to the bus system between bus and interface. This memory is occupied by sequences of control commands during phases that are not time critical. These command sequences are transferred to the interface in synchronism with the clocking of the peripheral associated with the interface. Two command decoders select the interface either directly or indirectly via the temporary storage of control words in the control word memory. The first decoder is between the control bus of the bus system, and the input of the control word memory.
The second decoder is between the output of the control word memory and a circuit located in the region of the interface. The system divides operations into immediately-executable operations and operations whose execution need not be immediate. i.e. the processor is only responsible for operations that are not critical as regards time, whereas time-critical operations are handled by the specialised control word memory.

Original Publication Data by Authority...**Claims:**and for switching the integrated memory device to a mode which is determined by the **control word**, and also comprises a **parallel**-in/parallel-out mode, each memory section having its own input terminal (MI) and output...

{** your application **}

21/5/1 (Item 1 from file: 350) **Links**
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0013475892 *Drawing available*
WPI Acc no: 2003-567685/200353
XRPX Acc No: N2003-451349
Data processing system, has control word logic that supplies control words having routing control signals to routing units that are coupled to functional units
Patent Assignee: KIZHEPAT G (KIZH-I); UNIVERSAL NETWORK MACHINES INC (UVNE-N)
Inventor: KIZHEPAT G

Patent Family (6 patents, 99 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20030088826	A1	20030508	US 2001992637	A	20011106	200353	B
WO 2003040952	A1	20030515	WO 2002US24815	A	20020805	200353	E
EP 1442393	A1	20040804	EP 2002752696	A	20020805	200451	E
			WO 2002US24815	A	20020805		
AU 2002363356	A1	20030519	AU 2002363356	A	20020805	200464	E
JP 2005508554	W	20050331	WO 2002US24815	A	20020805	200523	E
			JP 2003542509	A	20020805		
CN 1585939	A	20050223	CN 2002822223	A	20020805	200537	E

Priority Applications (no., kind, date): US 2001992637 A 20011106

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 20030088826	A1	EN	10	5		
WO 2003040952	A1	EN				
National Designated States,Original	AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW					
Regional Designated States,Original	AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SK SL SZ TR TZ UG ZM ZW					
EP 1442393	A1	EN			PCT Application	WO 2002US24815
					Based on OPI patent	WO 2003040952
Regional Designated States,Original	AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR					
AU 2002363356	A1	EN			Based on OPI patent	WO 2003040952
JP 2005508554	W	JA	32		PCT Application	WO 2002US24815
					Based on OPI patent	WO 2003040952

Alerting Abstract US A1
NOVELTY - The system has routing units (70-72) coupled to functional units (75-76). The routing units are responsive to routing control signals and enables **data steering** among the functional units. The routing control signals indicate a source functional unit and a destination functional unit for a data unit. A **control word** logic supplies **control words** having routing control signals to the routing units.
DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of processing data in a data processing engine.
USE - Used for performing operations and computations on data.

ADVANTAGE - The **control word** logic is flexible and can be used for any number of operations. The system is flexible and allows easy altering of its parameters even when the complexity of the system increases.
DESCRIPTION OF DRAWINGS - The drawing shows a simplified architectural diagram of a data processing system.
70-72 Routing units
75-76 Functional units.

NPL ABSTRACTS

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```
; d s
Set   Items   Postings  Description
S1      1326      3838  S CONTROL()WORD? ? OR ROUT???(2N)INSTRUCTION? ?
S2     10350     23216  S (ROUT??? OR STEER???)(2N)(UNIT? ? OR PART? ? OR APPARATUS OR APPTS
OR ELEMENT? ?)
S3         6        12  S FUNTIONAL(2N)(UNIT? ? OR PART? ? OR APPARATUS OR APPTS OR ELEMENT? ?)
S4   1112293   2546105  S (LOGIC? OR LOOKUP? OR LOOK()UP? ? OR SHIFT??? OR STORAGE)()(UNIT?
? OR PART? ? OR APPARATUS? OR APPTS OR ELEMENT? ?) OR ALU OR ALUS OR MEMORY OR
BUFFER? ?
S5        16        59  S S1(5N)(PARALLEL? OR SIMULTANEOUS? OR SAME()TIME)
S6     21814     53062  S S3:S4(3N)(CONFIGUR? OR SELECT? OR ARRANG? OR ORDER?)
S7        13        46  RD S5  (unique items)
S8        11        38  S S7 NOT PY=2002:2008
S9        15        80  S S1 AND S6
S10       12        68  RD  (unique items)
```

S11	10	60	S S10 NOT PY=2002:2008
S12	362	2450	S S1 AND (ROUTE? ? OR ROUTING OR STEER???)
S13	46	411	S S12 AND ARCHITECTURE? ?
S14	20	225	S S13 AND PARALLEL?
S15	16	174	S S14 NOT (S8 OR S11)
S16	14	158	S S15 NOT PY=2002:2008
S17	36	94	S DATA()STEERING
S18	22	60	RD (unique items)
S19	18	52	S S18 NOT PY=2002:2008

8/5/2 (Item 2 from file: 2) **Links**

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INSPEC

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07283678 **INSPEC Abstract Number:** B1999-08-4180-044, C1999-08-5270-041

Title: Reconfigurable processor employing optical channels

Author Sakr, M.F.; Levitan, S.P.; Giles, C.L.; Chiarulli, D.M.

Author Affiliation: Dept. of Electr. Eng., Pittsburgh Univ., PA, USA

Journal: Proceedings of the SPIE - The International Society for Optical Engineering **Conference Title:** Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3490 p. 564-7

Publisher: SPIE-Int. Soc. Opt. Eng ,

Publication Date: 1998 **Country of Publication:** USA

CODEN: PSISDG **ISSN:** 0277-786X

SICI: 0277-786X(1998)3490L.564:RPEO;1-A

Material Identity Number: C574-1998-150

U.S. Copyright Clearance Center Code: 0277-786X/98/$10.00

Conference Title: Optics in Computing '98

Conference Sponsor: SPIE; Eur. Opt. Soc.; Int. Commission for Opt.; IEEE/Lasers & Electro-Opt. Soc.; et al

Conference Date: 17-20 June 1998 **Conference Location:** Brugge, Belgium

Language: English **Document Type:** Conference Paper (PA); Journal Paper (JP)

Treatment: Practical (P); Theoretical (T); Experimental (X)

Abstract: A reconfigurable processor architecture is proposed that overcomes limitations by using high bandwidth optical channels. The optical channels allow fast **parallel** loading of the reconfiguration **control word** as well as the migration of the configuration cache off-chip. The migration of configuration cache allows better utilization of the die area for reconfigurable processing elements. Further, it is possible to implement the optical detectors directly in silicon, which does not require significant alteration of the fabrication processes. These advantages make the optically reconfigurable architecture competitive for high performance applications. (4 Refs)

Subfile: B C

Descriptors: field programmable gate arrays; optical logic; parallel architectures; photodetectors; reconfigurable architectures

Identifiers: optical channels; reconfigurable processor; high bandwidth optical channels ; fast parallel loading; reconfiguration control word; configuration cache off-chip migration; optical detectors; fabrication processes; reconfigurable architecture; high performance applications; optical computing; FPGA

Class Codes: B4180 (Optical logic devices and optical computing techniques); B1265B (Logic circuits); B7230C (Photodetectors); C5270 (Optical computing techniques); C5110D (Optical logic elements); C5220P (Parallel architecture)

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8/5/5 (Item 5 from file: 2) **Links**
INSPEC
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01190106 **INSPEC Abstract Number:** C70020642
Title: Communications control apparatus in an information processing system
Inventor Goshorn, L.A.; Harmon, S.A.
Assignee General Electric Co
Patent Number: US 3487370 **Issue Date:** 691230
Application Date: 661222
Priority Application Number: US 603943
Country of Publication: USA

Language: English **Document Type:** Patent (PT)
Abstract: After description of an information processing system, apparatus for providing communication between a memory unit and any one of a plurality of peripheral buffers thereof is related. A list command word in the arithmetic unit of the processing system includes a field specifying an address in the memory unit for a list control word and a field specifying a command to transfer an information item in a particular direction between a peripheral buffer and the list. The list control word provides four fields defining the current status of the list, including the maximum length, the number of items currently stored in the list, and whether the list is currently full or empty, and in addition provides a fifth field for developing the address of a storage location in memory of the beginning list item. In response to the command of the list command word, apparatus is provided to employ the fields of the list control word to develop by variable- modulo arithmetic the address of a particular storage location in memory with which a peripheral buffer is to communicate, and apparatus is provided to develop the address of a device code word specifying a particular peripheral buffer. From the device code, apparatus is provided to select a communication channel between the selected buffer and the selected storage location in memory and to transfer in response to the device command an information item therebetween. Furthermore, apparatus is provided to **simultaneously** update the list **control word** during exception of the list command and to restore it to memory.
Subfile: C
Descriptors: data communication systems
Class Codes: C5600 (Data communication equipment and techniques)

8/5/9 (Item 4 from file: 8) **Links**

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Ei Compendex(R)

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03404452 **E.I. Monthly No:** EI7410061013

Title: ERROR CHECKING AND CORRECTION OF MICROPROGRAM CONTROL WORDS WITH A LATE BRANCH FIELD.

Author: Healey, R. A.

Source: IBM Technical Disclosure Bulletin v 17 n 2 Jul 1974 p 374-381
Publication Year: 1974
CODEN: IBMTAA **ISSN:** 0018-8689
Language: ENGLISH
Journal Announcement: 7410

Abstract: Symmetrical error checking and correction (ECC) codes permit selection (by late branch address bits) without delay of one of N **control words** read **simultaneously** from control store with their ECC bits. Many systems in use today access two or more **control words simultaneously** from the control store, and one of these control words is selected by late branch circuits for use as the next control word, based upon the late branch information. Typically the ECC circuits are coupled directly to the output of the control store, but no check is made at the output of the control register to which the selected next control word is gated. Thus even though data read from the control store may be error free, nevertheless the output of the control store may contain an error. An arrangement is described here, however, in which the ECC circuitry is coupled to the output of the control register.

Descriptors: *COMPUTER ARCHITECTURE
Classification Codes:
723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

16/5/4 (Item 4 from file: 2) **Links**
INSPEC
(c) 2007 Institution of Electrical Engineers. All rights reserved.
05013282 **INSPEC Abstract Number:** C91070696
Title: Bidirectional, two dimensional regular data flow architecture
Author Almhana, J.
Author Affiliation: Dept. of Comput. Sci., Moncton Univ., NB, Canada
Conference Title: Supercomputing Symposium '91. Symposium Proceedings p. 399-407
Editor(s): Bhavsar, V.C.; Gujar, U.G.
Publisher: Univ. New Brunswick , Fredericton, NB, Canada
Publication Date: 1991 **Country of Publication:** Canada x+544 pp.
ISBN: 0 920114 14 8
Conference Date: 3-5 June 1991 **Conference Location:** Fredericton, NB, Canada

Language: English **Document Type:** Conference Paper (PA)
Treatment: Practical (P)
Abstract: The article describes a new, static, cellular data flow **architecture** with emphasis on its function mode and exchange means between cells; an algorithm is defined for **instruction** packet **routing**. It also defines the neighbouring concept and implementation rules which permit optimum mapping. (22 Refs)
Subfile: C
Descriptors: parallel architectures
Identifiers: bidirectional data flow **architecture**; static data flow **architecture**; two dimensional regular data flow **architecture**; cellular data flow **architecture**; function mode; exchange means; cells; **instruction** packet **routing**; neighbouring concept; implementation rules; optimum mapping
Class Codes: C5220 (Computer architecture)

16/5/12 (Item 2 from file: 35) **Links**
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01301365 ORDER NO: AADMM-73669
THE DESIGN OF PAAP: PROGRAMMABLE ASYNCHRONOUS ARRAY PROCESSOR

Author: ZELADA, MARCO A.
Degree: M.COMP.SC.
Year: 1992
Corporate Source/Institution: CONCORDIA UNIVERSITY (CANADA) (0228)
Source: Volume 31/03 of MASTERS ABSTRACTS. of Dissertations Abstracts International.
PAGE 1278 . 144 PAGES.
Descriptors: COMPUTER SCIENCE; ENGINEERING, ELECTRONICS AND ELECTRICAL
Descriptor Codes: 0984; 0544
ISBN: 0-315-73669-0

This thesis explores architectural features appropriate to massively **parallel architectures** such as, Processing Element (PE) and **Routing** Element (RE) programmability within an array processor environment, unrestricted data flow direction, and true array scalability. We illustrate these features through an array design, which we term the Programmable Asynchronous Array Processor (PAAP).

The PAAP proposes a methodology for mapping high-level computation into hardware structures. This feature is shared with systolic and wavefront arrays. However, the PAAP differs in that its PEs can be dynamically programmed to work in an MIMD fashion. They can also be interconnected via dyadic programmable REs to form asynchronous pipelines. In contrast, most systolic and wavefront arrays work in an SIMD fashion, have static interconnections and implement a single special purpose hard-wired instruction. Those which are programmable and work in an MIMD fashion lack the interconnection reconfigurability and data flow control present in the PAAP.

PE and RE instructions and data are not fetched from memory. Instead, the PE and RE are programmed to execute the desired **instruction** and **routing** scheme during the program load phase, and data flows through the complete array during the program execution phase. The essence of the **architecture** is captured by the configurable **routing** which gives the PAAP its flexibility and power. The RE is a four way bidirectional **router** which provides maximum flexibility in the definition of pipeline **routes**. It permits a pipeline to be defined in any direction across the array, downward, sideways in either direction, and upwards.

The PAAP addresses the three main asynchronous circuit problems, namely, computational interference, signal ordering, and transfer interference. It uses a modified two-phase protocol which allows the active and passive end of the circuit to implement their own return-to-zero synchronization upon the receipt of the proper protocol sequence (BrozozowskiJ89).

19/5/1 (Item 1 from file: 2) **Links**
INSPEC
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04976150 **INSPEC Abstract Number:** B91062083, C91057674
Title: Data path tradeoffs using MABAL
Author Kucukcakar, K.; Parker, A.C.
Author Affiliation: Dept. of Electr. Eng.-Syst., Univ. of Southern California, Los Angeles, CA, USA
Conference Title: 27th ACM/IEEE Design Automation Conference. Proceedings 1990 (Cat. No.90CH2894-4) p. 511-16
Publisher: IEEE , New York, NY, USA
Publication Date: 1990 **Country of Publication:** USA xxi+743 pp.
ISBN: 0 89791 363 9
U.S. Copyright Clearance Center Code: 0738-100X/90/0000-0511$1.00
Conference Sponsor: ACM; IEEE
Conference Date: 24-28 June 1990 **Conference Location:** Orlando, FL, USA

Language: English **Document Type:** Conference Paper (PA)
Treatment: Practical (P)
Abstract: A set of novel tradeoff experiments using MABAL, a module and bus allocation program, is described. MABAL uses a simple heuristic algorithm to concurrently perform functional unit allocation, register allocation, interconnect allocation, and module binding, while minimizing overall cost. MABAL was used to produce over 3000-RTL (register transfer level) designs from a specification which had been previously scheduled. Tradeoffs between buses and multiplexers and between **data steering** logic and functional logic were investigated. The results indicate that data path tradeoffs were sensitive to the characteristics of the module library used, and illustrate the difficulty of integrating module generations or logic synthesis, with high-level synthesis. (9 Refs)
Subfile: B C
Descriptors: heuristic programming; logic CAD
Identifiers: module and bus allocation program; heuristic algorithm; functional unit allocation; register allocation; interconnect allocation; module binding; register transfer level; multiplexers; **data steering** logic; functional logic; logic synthesis
Class Codes: B1265B (Logic circuits); C5210B (Computer-aided logic design); C1230 (Artificial intelligence)

19/5/2 (Item 2 from file: 2) **Links**

Fulltext available through: [USPTO Full Text Retrieval Options] STIC Full Text Retrieval Options

INSPEC

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04375877 **INSPEC Abstract Number:** B89036937, C89032543

Title: A systolic architecture for fast dense matrix inversion

Author El-Amawy, A.

Author Affiliation: Dept. of Electr. & Comput. Eng., Louisiana State Univ., Baton Rouge, LA, USA

Journal: IEEE Transactions on Computers vol.38, no.3 p. 449-55

Publication Date: March 1989 **Country of Publication:** USA

CODEN: ITCOB4 **ISSN:** 0018-9340

U.S. Copyright Clearance Center Code: 0018-9340/89/0300-0449$01.00

Language: English **Document Type:** Journal Paper (JP)

Treatment: Practical (P)

Abstract: An array that inverts an n*n dense matrix in 5n-1 time units, including I/O time, is presented. The inversion algorithm consists of three phases and assumes that Gaussian elimination without pivoting can be applied. The array, which consists of 2n/sup 2/-n simple processing elements, implements and overlaps the execution of all three phases without any need for intermediate I/O or reconfiguration. An efficient **data- steering** technique which is well suited for feedback recurrences is utilized. (12 Refs)

Subfile: B C

Descriptors: cellular arrays; computerised signal processing; VLSI

Identifiers: VLSI algorithms; systolic architecture; fast dense matrix inversion; Gaussian elimination; **data-steering** technique; feedback recurrences

Class Codes: B1265B (Logic circuits); B2570 (Semiconductor integrated circuits); C5260 (Digital signal processing); C5120 (Logic and switching circuits)

19/5/3 (Item 3 from file: 2) **Links**

Fulltext available through: Click to Full Text Knovel Options STIC Full Text Retrieval Options

INSPEC

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04150693 **INSPEC Abstract Number:** B88040886, C88034697

Title: A systolic architecture for optimal filter design support

Author El-Amawy, A.

Author Affiliation: Dept. of Electr. & Comput. Eng., Louisiana State Univ., Baton Rouge, CA, USA

Journal: Circuits, Systems, and Signal Processing vol.7, no.2 p. 151-72

Publication Date: 1988 **Country of Publication:** USA

CODEN: CSSPEH **ISSN:** 0278-081X

Language: English **Document Type:** Journal Paper (JP)

Treatment: Theoretical (T)

Abstract: A prototype filter design is reviewed to underscore the computational problems arising in such designs. A purely systolic-array architecture is presented. This array provides the computational support necessary for filter design., Due to a simple and novel **data steering** technique the array is capable of carrying out a number of important matrix operations such as factorization, inversion of factors, and matrix-matrix multiplication. Another interesting attribute is the array's ability to maximally overlap computations of multiphase algorithms. In this study the author demonstrates the execution of a dense matrix factorization phase and factor inversion phase on the array with no need for intraphase or interphase I/O. He shows that these phases (which are the backbone of an optimal filtering algorithm) are completed in the optimal count of about 4n time units. The array employs 2n/sup 2/-n simple processing elements (PEs) that are active every other time unit. It is shown that the functions of two adjacent PEs can be merged and assigned to a single PE thus maximizing PE utilization. A possible design of a 'merged' PE is given. (17 Refs)

Subfile: B C

Descriptors: cellular arrays; digital filters; filtering and prediction theory; matrix algebra; optimisation; parallel architectures

Identifiers: systolic array; intraphase I/O; systolic architecture; optimal filter design support; **data steering** technique; matrix operations; factorization; matrix-matrix multiplication; multiphase algorithms; factor inversion phase; interphase I/O; processing elements

Class Codes: B0260 (Optimisation techniques); B1265B (Logic circuits); B1265D (Memory circuits); B6140 (Signal processing and detection); C1180 (Optimisation techniques); C1260 (Information theory); C5220 (Computer architecture); C5240 (Digital filters)

19/5/4 (Item 4 from file: 2) **Links**

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INSPEC

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04022244 **INSPEC Abstract Number:** B88000848, C88001889

Title: Solution of dense linear systems on an optimal systolic architecture

Author El-Amawy, A.

Author Affiliation: Dept. of Electr. & Comput. Eng., Louisiana State Univ., Baton Rouge, LA, USA

Journal: Computers & Electrical Engineering vol.13, no.3-4 p. 177-93

Publication Date: 1987 **Country of Publication:** USA

CODEN: CPEEBQ **ISSN:** 0045-7906

U.S. Copyright Clearance Center Code: 0045-7906/87/$3.00+0.00

Language: English **Document Type:** Journal Paper (JP)

Treatment: Practical (P); Theoretical (T)

Abstract: The paper presents an optimal systolic array architecture for rapid solution of dense systems of linear equations. The array solves a system of size nxn in 4n+1 time units including I/0 time. Data communications are strictly local and the processing elements (PEs) are simple. The complete three-phase solution algorithm is executed on a single array, employing about 3n/sup 2//2 PEs without any need for costly inter-phase I/0. Due to a novel **data steering** mechanism, the three algorithmic phases are maximally overlapped. Design optimality is established using systolic precedence diagrams. It is also shown that merging the functions of two adjacent PEs into a single PE is possible resulting in maximal PE utilization. An interesting result regarding cascading phase-optimal arrays is obtained. (22 Refs)

Subfile: B C

Descriptors: cellular arrays; linear systems; parallel algorithms; parallel architectures

Identifiers: direct solution; dense linear systems; optimal systolic architecture; systolic array architecture; dense systems of linear equations; three-phase solution algorithm; **data steering** mechanism; systolic precedence diagrams; phase-optimal arrays

Class Codes: B1265Z (Other digital circuits); C4140 (Linear algebra); C5220 (Computer architecture); C7310 (Mathematics)

19/5/5 (Item 5 from file: 2) **Links**
INSPEC
(c) 2007 Institution of Electrical Engineers. All rights reserved.
03987338 **INSPEC Abstract Number:** C87059518
Title: High speed inversion of dense matrices on an optimal systolic array
Author El-Amawy, A.
Author Affiliation: Dept. of Electr. & Comput. Eng., Louisiana State Univ., Baton Rouge, LA, USA
Conference Title: Proceedings of VLSI and Computers. First International Conference on Computer Technology, Systems and Applications. COMPEURO 87 (Cat. No.87CH2417-4) p. 707-11
Editor(s): Proebster, W.E.; Reiner, H.
Publisher: IEEE Comput. Soc. Press , Washington, DC, USA
Publication Date: 1987 **Country of Publication:** USA xvii+1006 pp.
ISBN: 0 8186 0773 4
U.S. Copyright Clearance Center Code: CH2417-4/87/0000-0707$01.00
Conference Sponsor: IEEE; Gesellschaft Inf.; Verband Deutscher Elektrotech
Conference Date: 11-15 May 1987 **Conference Location:** Hamburg, West Germany

Language: English **Document Type:** Conference Paper (PA)
Treatment: Practical (P)
Abstract: An optimal systolic array architecture for fast inversion of dense matrices is presented. The array inverts an n*n dense matrix in 5n-1 time units which includes I/O time. The array uses 2n/sup 2/-n simple processing elements (PEs) arranged in an (2n-1)*n rectangle. The PEs are active every other time unit. Data communications are strictly local, and no intermediate I/O is required. A novel **data-steering** mechanism that is well suited for feedback recurrencies is utilized. Design optimality is established using systolic precedence diagrams. It is shown that cascading phase-optimal arrays does not necessarily result in an algorithm-optimal design. (8 Refs)
Subfile: C
Descriptors: parallel architectures
Identifiers: high speed inversion; data communications; dense matrices; optimal systolic array; architecture; **data-steering** mechanism; feedback recurrencies
Class Codes: C5220 (Computer architecture); C5440 (Multiprocessor systems and techniques)

19/5/6 (Item 6 from file: 2) **Links**
INSPEC
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03125086 **INSPEC Abstract Number:** C83038561
Title: Large system fault tolerant memory techniques
Author RYAN, P.M.
Author Affiliation: IBM General Technol. Div., East Fishkill, NY, USA
Conference Title: FTCS 13th Annual International Symposium. Fault-Tolerant Computing. Digest of Papers p. 342-5
Publisher: IEEE , New York, NY, USA
Publication Date: 1983 **Country of Publication:** USA xxxv+490 pp.
U.S. Copyright Clearance Center Code: 0731-3071/83/0000/0342$01.00
Conference Sponsor: IEEE
Conference Date: 28-30 June 1983 **Conference Location:** Milan, Italy

Language: English **Document Type:** Conference Paper (PA)
Treatment: Practical (P)
Abstract: A memory served by single-bit error checking and correction (ECC) logic may be substantially improved by providing it with address-permutation and/or **data-steering** logic which rearranges patterns of faults uncorrectable by ECC into patterns which are correctable. An extension of ECC is described which both recovers the correct data from uncorrectable words and identifies the array chips which caused the error. An algorithm is described which uses this and other fault identification data to control the steering logic. The algorithm makes use of the fact that certain types of array faults are 'compatible' and may serve the same set of memory words without aligning in any one ECC word. It is shown that this approach leads to a memory structure which may tolerate many dozens of array failures without requiring repair. (13 Refs)
Subfile: C
Descriptors: error correction; fault tolerant computing; logic testing; semiconductor storage
Identifiers: large system fault tolerant memory techniques; error correction; fault location; single-bit error checking; address-permutation; **data- steering** logic
Class Codes: C5210 (Logic design methods); C5320G (Semiconductor storage)

19/5/7 (Item 7 from file: 2) **Links**

Fulltext available through: STIC Full Text Retrieval Options

INSPEC

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02897155 **INSPEC Abstract Number:** B82040283, C82030585

Title: Memory data steering using on-chip switching network and off-chip control network

Author Cavaliers, J.R.; Desai, S.; Eardley, D.B.; Feinberg, I.; Repchick, D.P.

Author Affiliation: IBM Corp., Armonk, NY, USA

Journal: IBM Technical Disclosure Bulletin vol.24, no.9 p. 4779-81

Publication Date: Feb. 1982 **Country of Publication:** USA

CODEN: IBMTAA **ISSN:** 0018-8689

Language: English **Document Type:** Journal Paper (JP)

Treatment: New Developments (N)

Abstract: Uses a laser delete link facility on the module to provide static signal inputs to the memory chip in order to control circuits effecting the replacement of defective bit positions. (0 Refs)

Subfile: B C

Descriptors: redundancy; semiconductor storage

Identifiers: memory **data steering**; memory chips; on-chip switching network ; off-chip control network; laser delete link facility; replacement of defective bit positions

Class Codes: B1265D (Memory circuits); C5320G (Semiconductor storage)

19/5/14 (Item 1 from file: 8) **Links**

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Ei Compendex(R)

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04550730 **E.I. Monthly No:** EI8408075064 **E.I. Yearly No:** EI84020338

Title: TWO-TIER ERROR CORRECTION CODE FOR MEMORIES.

Author: Wortzman, D.

Source: IBM Technical Disclosure Bulletin v 26 n 10A Mar 1984 p 5314-5318

Publication Year: 1984

CODEN: IBMTAA **ISSN:** 0018-8689

Language: ENGLISH

Journal Announcement: 8408

Abstract: The correction ability of single error correct and double error detect (SEC/DEC) codes is improved by partitioning the memory into two regions of ECC bit positions. One region has greater than nominal correctability into which known faulty memory bits are mapped by address or **data steering**. The other region has less than nominal correctability into which no known faulty memory bits are mapped. Conventional error correcting codes (ECCs) treat all bits of an ECC word in the same manner. A code is described which is very correctable for a few of the bits and is much less correctable for the remainder of the bits. By logically moving all known faulty bits to the high correctability region, the overall correctability of the code is improved. No additional bits are required over conventional SEC/DET codes.

Descriptors: *CODES, SYMBOLIC--*Error Correction; DATA STORAGE, DIGITAL

Classification Codes:

723 (Computer Software); 721 (Computer Circuits & Logic Elements); 722 (Computer Hardware)

72 (COMPUTERS & DATA PROCESSING)

19/5/15 (Item 2 from file: 8) Links

Fulltext available through: USPTO Full Text Retrieval Options STIC Full Text Retrieval Options

Ei Compendex(R)

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04542190 **E.I. Monthly No:** EI8407064304 **E.I. Yearly No:** EI84031772

Title: DYNAMIC DECODER FOR MULTIPLE SPARES AND SELECT REDISTRIBUTION WITHIN A SELECT PARTITION.

Author: Aichelmann, F. J. Jr.

Source: IBM Technical Disclosure Bulletin v 26 n 6 Nov 1983 p 2759-2761
Publication Year: 1983
CODEN: IBMTAA **ISSN:** 0018-8689
Language: ENGLISH
Journal Announcement: 8407

Abstract: Fault-tolerant techniques are used in memory systems to minimize the accumulation of faults which would otherwise result in unusable memory locations. These techniques involve sparing, **data steering**, or address reconfiguration for the dispersion of defects so that they do not accumulate within the same ECC word. A technique is pointed out where sparing and reconfiguration can be combined across a selection partition by the use of an M/N decoder instead of an I/N decoder.

Descriptors: *DATA STORAGE, DIGITAL--*Failure
Classification Codes:
721 (Computer Circuits & Logic Elements); 722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING)

19/5/17 (Item 1 from file: 35) **Links**
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01637170 ORDER NO: AAD98-26715
VISUAL ASSISTANCE FOR CONCURRENT PROCESSING (DEBUGGING)

Author: ERBACHER, ROBERT F.
Degree: D.SC.
Year: 1998
Corporate Source/Institution: UNIVERSITY OF LOWELL (0111)
Supervisor: GEORGES G. GRINSTEIN
Source: Volume 5903B of Dissertations Abstracts International.
PAGE 1196 . 203 PAGES
Descriptors: COMPUTER SCIENCE
Descriptor Codes: 0984

Recent advances in concurrent architecture technology have led to a dramatic increase in the number of types of systems available as well as the number of systems in actual use. In contrast, software technology has not kept pace. Software tools have yet to be developed which fully compensate for the added difficulties and complexities inherent in programming concurrent architectures. Consequently, the tools used to aid in the development and debugging of applications for these types of architectures are often insufficient for the task. This makes it extremely difficult and time consuming to develop correct and efficient concurrent applications. The availability of high end graphics systems with most concurrent hardware provides an opportunity to extend development and debugging tools to use these graphics capabilities, where applicable.

In this research, we explored interactive computational steering, data analysis (as opposed to processor or control analysis), analysis of data operations, often using direct manipulation techniques, all in support of the development of concurrent applications.

We extended interactive computational steering beyond the ability to merely steer data values instantaneously. This resulted in techniques for the steering of operations, allowing the user to modify the application dynamically during execution. We also extended **data steering** to incorporate a persistent mode. In the persistent mode, once the user has specified the values for designated variable elements, the environment does not allow them to change.

Operation visualization techniques that are merged with the data display provide the user with a single focus and aid in the correlation of data, program status, and loop status information. The environment presents the operation visualizations in such a way that the user can also use them to debug the execution stack.

Finally, we show how users can apply the techniques developed during the course of this research to aid in the comprehension and debugging of concurrent programs. Examples show how the techniques can be used to find potential errors in two example concurrent applications or to verify that errors do not exist.

STIC SEARCH NOTES
(LAST PAGE)

19/5/18 (Item 2 from file: 35) **Links**
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01302532 ORDER NO: AADMM-75558

A SYNERGISTIC SCHEDULING, ALLOCATION, AND BINDING APPROACH IN BEHAVIORAL SYNTHESIS

Author: MUKHERJEE, NILANJAN
Degree: M.SC.
Year: 1992
Corporate Source/Institution: UNIVERSITY OF GUELPH (CANADA) (0081)
Source: Volume 31/03 of MASTERS ABSTRACTS. of Dissertations Abstracts International.
PAGE 1271 . 135 PAGES
Descriptors: COMPUTER SCIENCE
Descriptor Codes: 0984
ISBN: 0-315-75558-X

Behavioral-level datapath synthesis has two major aspects. The first is operational optimization, that concerns three independent tasks: (i) allocating a set of functional units to the design; (ii) scheduling operations on control steps; and (iii) associating the operations with functional units on which they will execute, a process called binding. The other, known as storage and interconnect optimization, is responsible for allocating intermediate storage and **data steering** elements necessary for implementation of a design. In this thesis, we provide an integrated and globally optimum solution for the subtasks of operational optimization.

The solution utilizes an integer linear program (ILP) that minimizes a weighted sum of module area and total execution time under very general assumptions of module capability. In particular, a module may execute an arbitrary combinations of operations, possibly using different numbers of control steps for different operations. Furthermore, operations may be implemented by a variety of modules, possibly requiring different number of control steps depending on the modules chosen. This generality in the complexity and mixture of functional units is unique to our system.

We also show how our model is extended to consider several other aspects, such as, chaining, structural pipelining, and inclusion of an interconnection estimate. The model is also applied to synthesize multiple control block designs, where all the blocks are considered simultaneously.